

FIG. 4

Block diagram of a digital filter circuit 105. The circuit has two inputs: $I_1' \text{ OR } Q_1'$ and $I_2 \text{ OR } Q_2$. The $I_1' \text{ OR } Q_1'$ input is connected to a multiplexer 72, which selects between a feedback signal $X(n)$ and a new input signal $X(n-1)$ from a REGISTER. The output of multiplexer 72 is $X(n)$, which is also the output of the circuit. $X(n)$ is fed into a summing junction 82, which also receives a feedback signal from the output of a multiplier 86. The output of summing junction 82 is Y . Y is fed into multiplier 86, which also receives a coefficient b from a memory block 74. The output of multiplier 86 is fed back to summing junction 82. Y is also fed into a second summing junction 90, which also receives a feedback signal from the output of a multiplier 92. The output of summing junction 90 is $Y(n)$, which is the output of the circuit. $Y(n)$ is also fed into multiplier 92, which also receives a coefficient a from a memory block 84. The output of multiplier 92 is fed back to summing junction 90. The circuit is controlled by a SAMPLE CLOCK and a BCLK signal.

